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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,913	10/01/2003	Dennis M. O'Connor	P17474	9573

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EXAMINER	
ZHE, MENG YAO	
ART UNIT	**PAPER NUMBER**
2109	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/677,913	O'CONNOR ET AL.	
	Examiner	Art Unit	
	MengYao Zhe	2109	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 to 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 to 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/21/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is the initial office action based on the 10/677913 application filed on 10/1/2003.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 3/21/2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 10 recites the limitation "the non-executing thread" in lines 21 to 22. There is insufficient antecedent basis for this limitation in the claim. It is unclear as to whether "the none-executing thread" is the "non-executing thread" mentioned in line 20 of claim 10 or the "one other non-executing thread" mentioned in line 21 of claim 10.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 to 5, 7, 9, 10 to 19, 20, and 22 to 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Horvitz Patent No. 6,009,452, 12/28/1999 (hereafter Horvitz).

As per **claim 1**, Horvitz teaches **a method, comprising:**

> **enabling execution of a non-executing thread based at least on whether a hardware resource is or will be available to an instruction of the non-executing thread.** *(Column 8, lines 20 to 21; Column 9, lines 5 to 66: Horvitz defines that a task is a equivalent of a thread. Horvitz teaches a method that executes waiting tasks during low CPU utilization, which happens when an executing task is waiting for another resource to become available.)*

As per **claim 13**, it claims for an article that comprises all the instructions necessary to perform the method of claim 1. Since claim 1 is rejected, claim 13 is rejected as well.

As per **claim 2**, Horvitz teaches

> **further comprising switching from the execution of a thread executing an instruction with long or potentially long latency, to the execution of the non-executing thread if the hardware resource is or will be available to the instruction of the non-executing thread.** *(Column 9, lines 5 to 66: during idle time, when a current executing task is waiting on another resource, Horvitz's invention would bring in a pending task for execution in order to utilize the CPU down times.)*

As per **claim 14**, it claims for an article that comprises all the instructions necessary to perform the method of claim 2. Since claim 2 is rejected, claim 14 is rejected as well.

As per **claim 3**, Horvitz teaches

> **further comprising switching from the execution of an executing thread to the execution of the non-executing thread if the hardware resource is or will be available to the instruction of the non-executing thread.** *(Column 9, lines 5 to 66)*

As per **claim 15**, it claims for an article that comprises all the instructions necessary to perform the method of claim 3. Since claim 3 is rejected, claim 15 is rejected as well.

As per **claim 4**, Horvitz teaches

comprising determining whether the hardware resource is or will be available to the instruction of the non-executing thread. *(Column 9, lines 5 to 66: the system disclosed by Horvitz know that when the CPU is idle, it should consider executing another more useful task.)*

As per claim 5, Horvitz teaches wherein determining comprises:

examining an instruction stream of the non-executing thread; identifying the instruction in the instruction stream; and *(Column 9, lines 5 to 66 and column 10: it is inherent that the tasks instances are examined in order to determined which one to pick for executing during idle time.)*

identifying hardware resources associated with the instruction, wherein examining occurs during execution of the executing thread. *(Abstract, last sentence)*

As per **claim 7**, Horvitz teaches

> **wherein enabling comprises enabling execution of the non-executing thread based on whether a functional unit is or will be available to the instruction of the non-executing thread** *(Column 9: The CPU is a functional unit.)*

As per **claim 9**, Horvitz teaches

> **enabling execution of a second non-executing thread if the hardware resource is available to the instruction of the non-executing thread** *(Column 10, lines 5 to 30: All unexecuted task instances may be executed. Only the one with higher probability will be executed sooner than the one with the lower probability.)*

As per **claim 10**, Horvitz teaches

> **further comprising switching from executing at least two executing threads to executing the non-executing thread and at least one other non-executing thread if the hardware resource is available to the instruction of the non-executing thread.** *(Column 10, lines 5 to 30: The Examiner has interpreted*

claim 10 as switching execution of two threads to execution of two other waiting threads. The Examiner also points out that true, complete concurrent execution of threads is impossible. Horvitz discloses idle time of CPU while other tasks are waiting. Therefore any tasks that are waiting are considered to be the executing threads. All unexecuted task instances may be executed. Only the one with higher probability will be executed sooner than the one with the lower probability. So two task instances I's are considered to be the two waiting threads.)

As per **claim 11**, Horvitz teaches **a method, comprising:**

switching from a first executing thread to a first pending thread based at least on the number of hardware resources unavailable to the first pending thread. *(Column 9, lines 20 to 30)*

As per **claim 12**, Horvitz teaches

determining the number of hardware resources unavailable to a second pending thread and wherein switching comprises switching from the first executing thread to the first pending thread if the number of unavailable hardware resources to the first pending thread is less than the number of unavailable hardware resources to the second pending thread. *(Column 11, lines 40 to 60, Column 14, lines 25 to 60: Horvitz teaches signing priorities to*

waiting tasks based on delayed future availability and how dependent the tasks are. As of result, those pending task with a less wait time, thus a higher priority, gets executed before those with a lower priority.)

As per **claim 16**, Horvitz teaches

A hardware resource *(Figure 5, unit 540 and 590 are all examples)*

A thread dispatch circuit. *(Figure 6, unit 630)*

Similarly, **claims 17 to 18, 20 and 22 to 24** are rejected.

As per **claim 19**, Horvitz teaches a CPU as a resource. Since every CPU contains an ALU and a register, it is inherent that that the hardware resource is ALU.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horvitz Patent No. 6,009,452, 12/28/1999 (hereafter Horvitz), in view of Budde et al., Patent No. 4,891,753, 1/2/1990.

As per **claim 6**, Horvitz teaches all of claim 1.

Horvitz does not teach

wherein enabling comprises enabling execution of the non-executing thread based on whether the hardware resource is scoreboarded.

However Budde teaches

> **enabling execution of the non-executing thread based on whether the hardware resource is scoreboarded** for the purpose of not wasting idle times of a resource. *(Column 1)*

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to have modified the invention of Horvitz with

> **enabling execution of the non-executing thread based on whether the hardware resource is scoreboarded,**

as taught by Budde, because idle times of a resource would not be wasted this way.

As per **claim 8**, Horvitz teaches all of claim 1 and

> **enabling execution of the non-executing thread if the hardware resource is available to the instruction of the non-executing thread**

Horvitz does not specifically specify

> **not enabling execution of the non-executing thread if the hardware resource is unavailable to the instruction of the non-executing thread.**

However, Budde teaches

> **not enabling execution of the non-executing thread if the hardware resource is unavailable to the instruction of the non-executing thread for the purpose of** not wasting idle times of a resource. *(Column 1)*

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to have modified the invention of Horvitz with

not enabling execution of the non-executing thread if the hardware resource is unavailable to the instruction of the non-executing thread

as taught by Budde, because idle times of a resource would not be wasted this way.

Claim 21 is rejected uner 35 U.S.C. 103(a) as being unpatentable over Horvitz.

As per **claim 21**, Horvitz teaches all of claim 16 and a look up table, which is the equivalent of a register lookup . Horvitz is silent to the apparatus of claim 16 having specifically

an instruction cache,

instruction decoder,

a register lookup.

However, Horvitz does disclose a CPU (Figure 5, unit 540). It is well-known and recognized in the art that an instruction cache is used in a CPU to bring up instructions for execution.

Horvitz also discloses an operating system (Figure 6, unit 610). It is well-known and recognized in the art that a register lookup is used in an operating system to bring up data and instructions for execution.

Horvitz also discloses a word processing program (Column 24, line 39) as an example of a task. It is well-know and recognized in the art that a word processing program is written with higher programming language, and in order to be ultimately executed, a compiler is needed to compile a higher language program into lower machine language. The Examiner has considered the compiler to be an instruction decoder.

Claims 25 to 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horvitz Patent No. 6,009,452, 12/28/1999 (hereafter Horvitz), in view of Dukach et al., Pub No. US 2004/0036622, 2/26/2004 (hereafter Dukach).

As per **claim 25**, Horvitz teaches

A processor *(Figure 5, unit 540)*

A hardware resource *(Figure 5, unit 540 and 590 are all examples)*

A thread dispatch circuit. *(Figure 6, unit 630)*

Horvitz does not teach an antenna.

However, Dukach teaches **a wireless phone with an antenna** *(Figure 18, unit 340 and 342)* **with a processor** for the purpose of controlling the execution of various tasks for the cell phone *(Paragraph 161)*

It would have been obvious to one having ordinary skill in the art at the time o the applicant's invention to have employed the invention of Horvitz on a cell phone with an antenna, as taught by Dukach, because it allows for the control over the execution of various tasks for the cell phone.

Similarly, **claims 26 and 27** are rejected as well.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MengYao Zhe whose telephone number is 571-272-6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Del Sole can be reached on 571-272-1130. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

M.Z.

Kim Nguyen

Kimberly Nguyen
Primary Examiner